

The diagram illustrates the interconnections of a computer system's memory and processing components. At the top, a horizontal bus line connects to two memory blocks: **Programmable Memory 14** on the left and **Read Only Memory 16** on the right. Below these, a **Memory Controller 12** is connected to the bus. The Memory Controller is also connected to a **Processor 10** block at the bottom. A **latch 18** (labeled with S, Q, R, and \overline{Q} inputs/outputs) is connected to the Memory Controller and the Processor. The latch's **Q** output is connected to the Memory Controller, and its **\overline{Q}** output is connected to the Processor's **Access Latch Reset** input. The latch's **S** (Set) input is connected to a **Power On Reset** signal, and its **R** (Reset) input is connected to the Processor's **Reset** input.

Figure 1

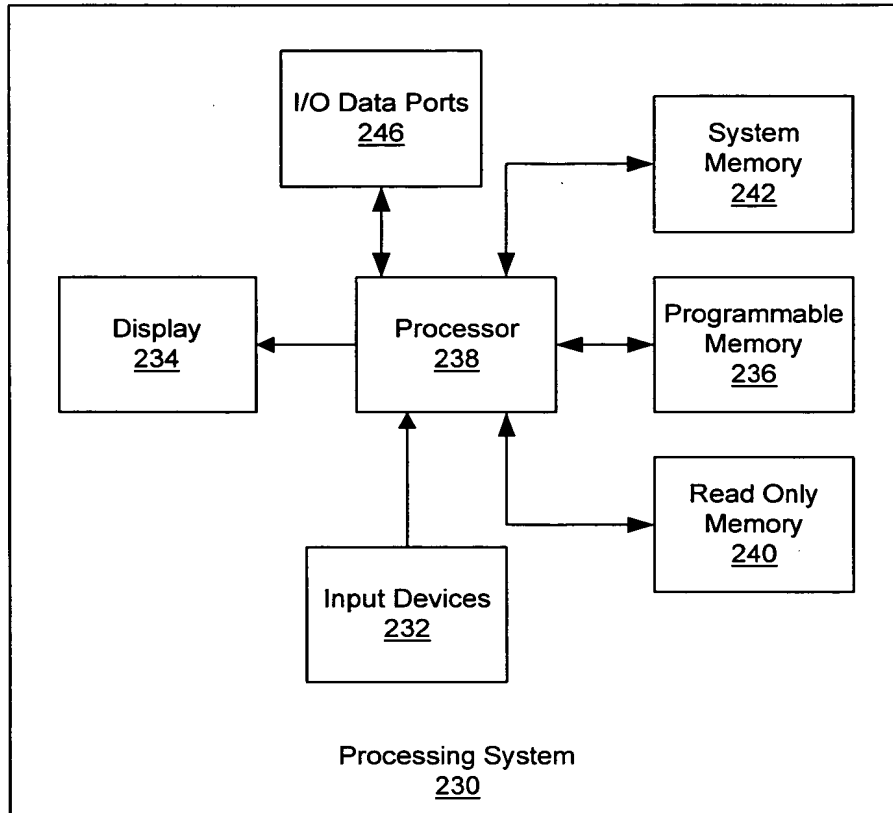


Figure 2

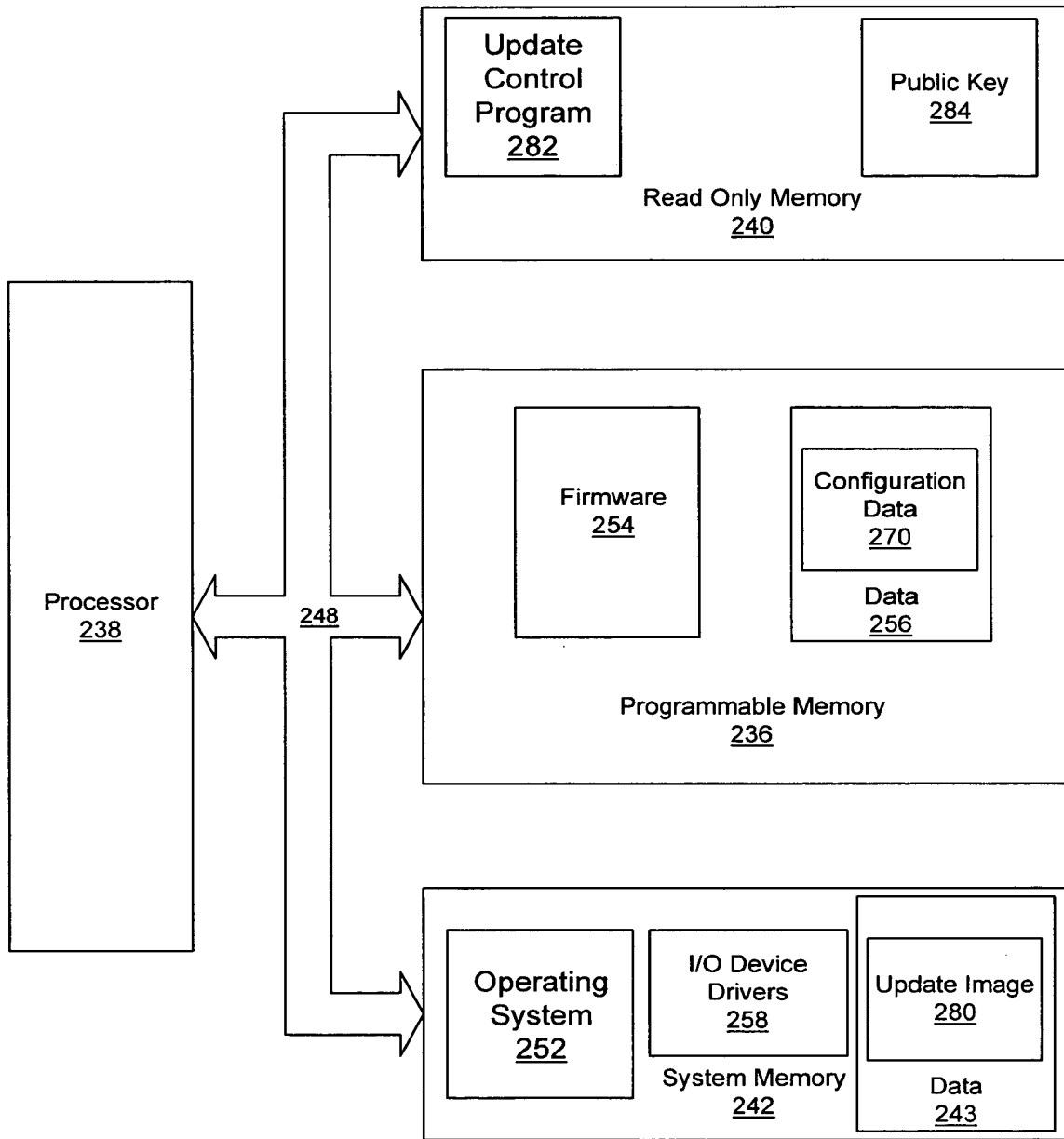


Figure 3

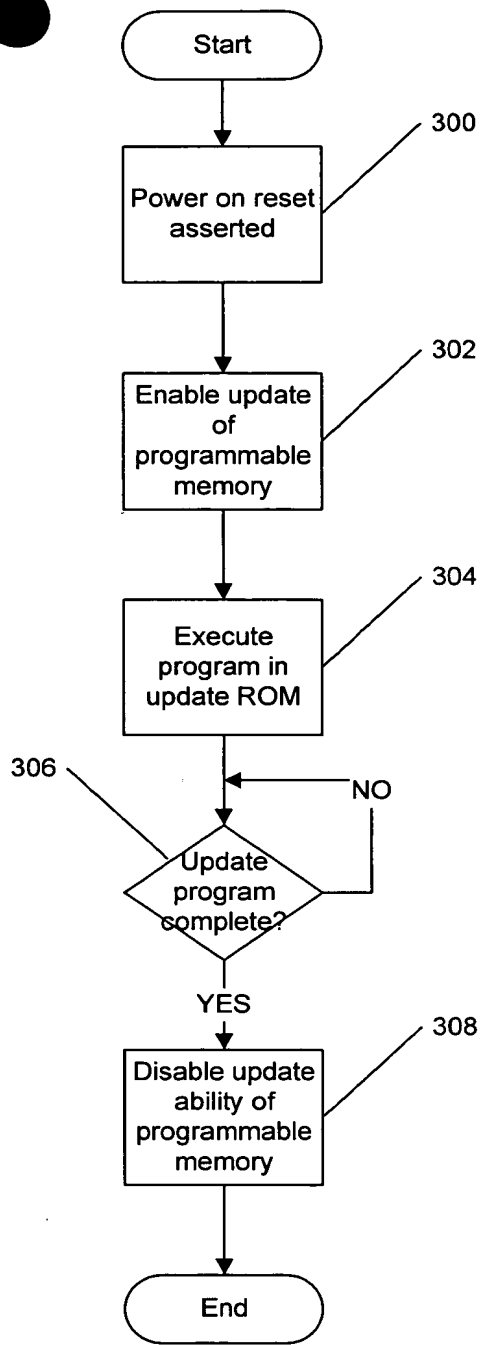


Figure 4A

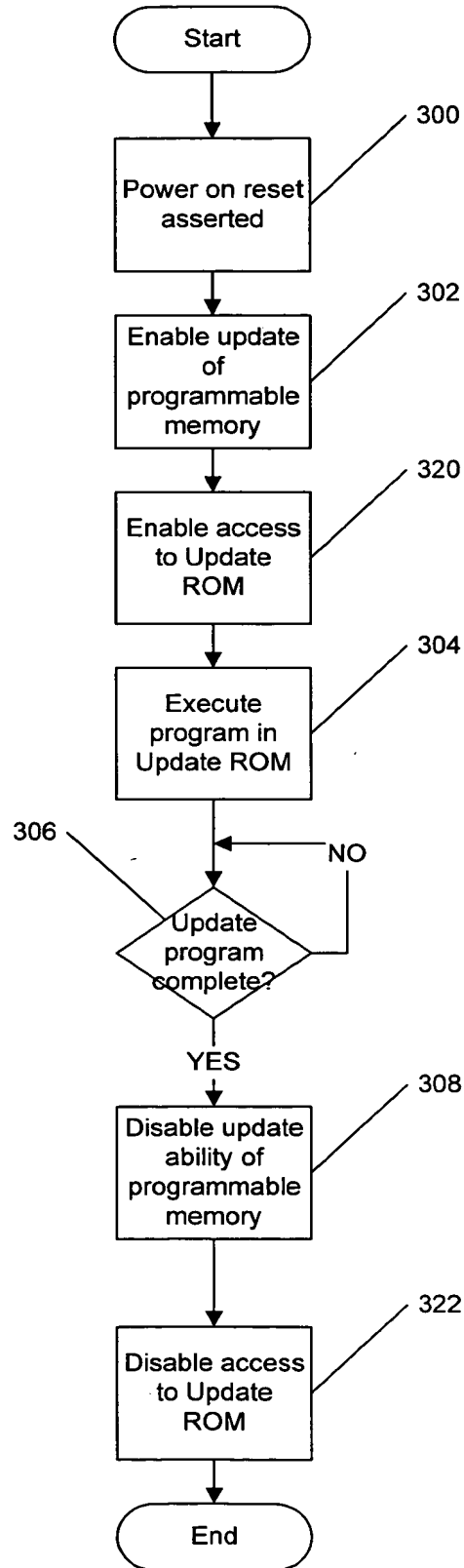
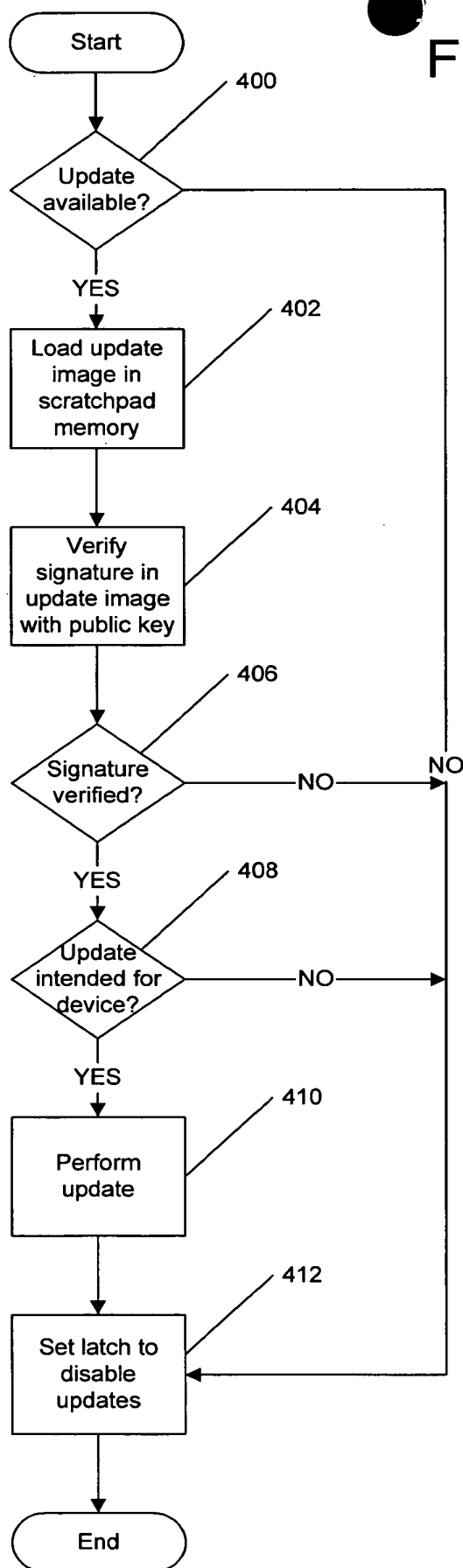
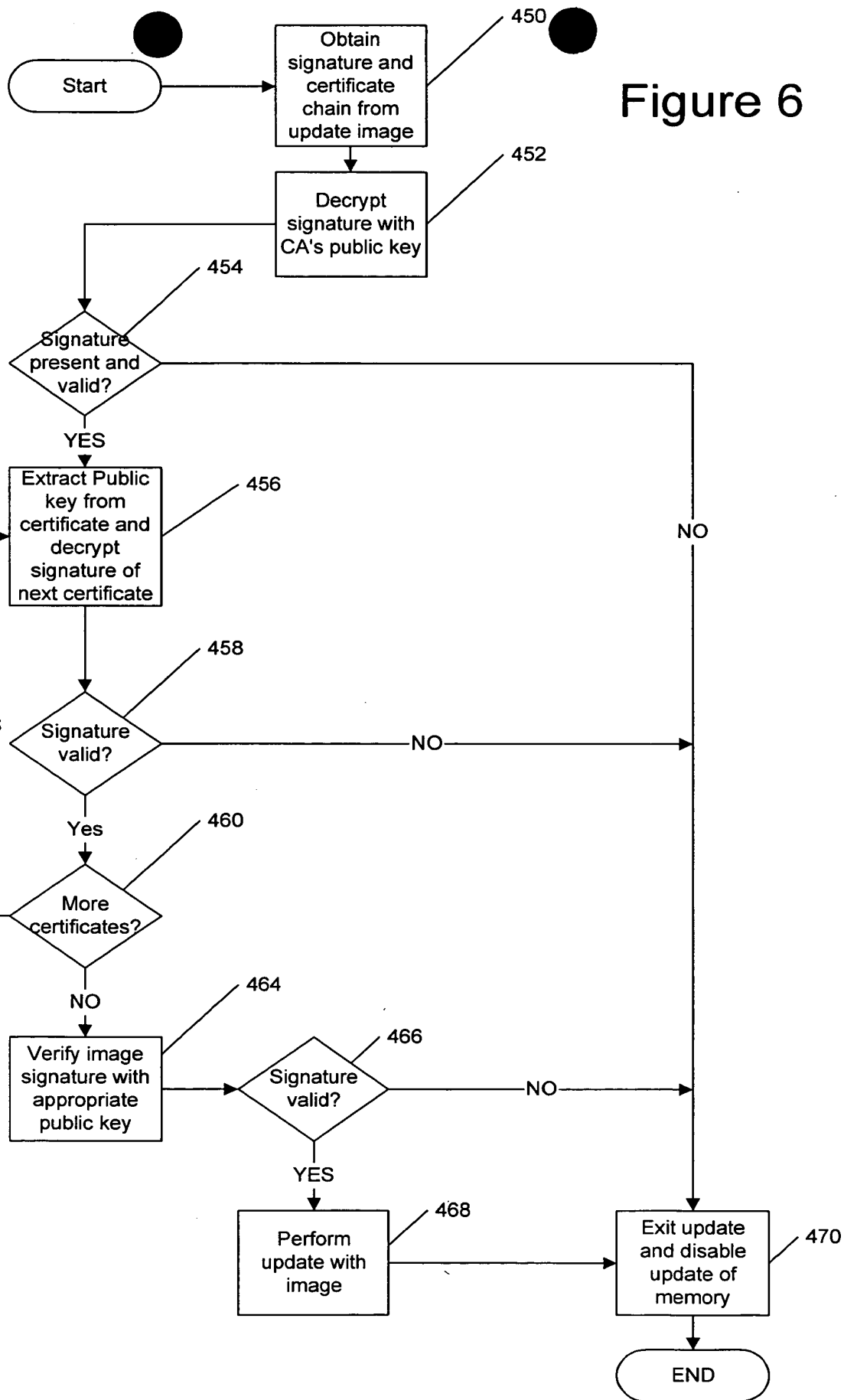


Figure 4B

Figure 5





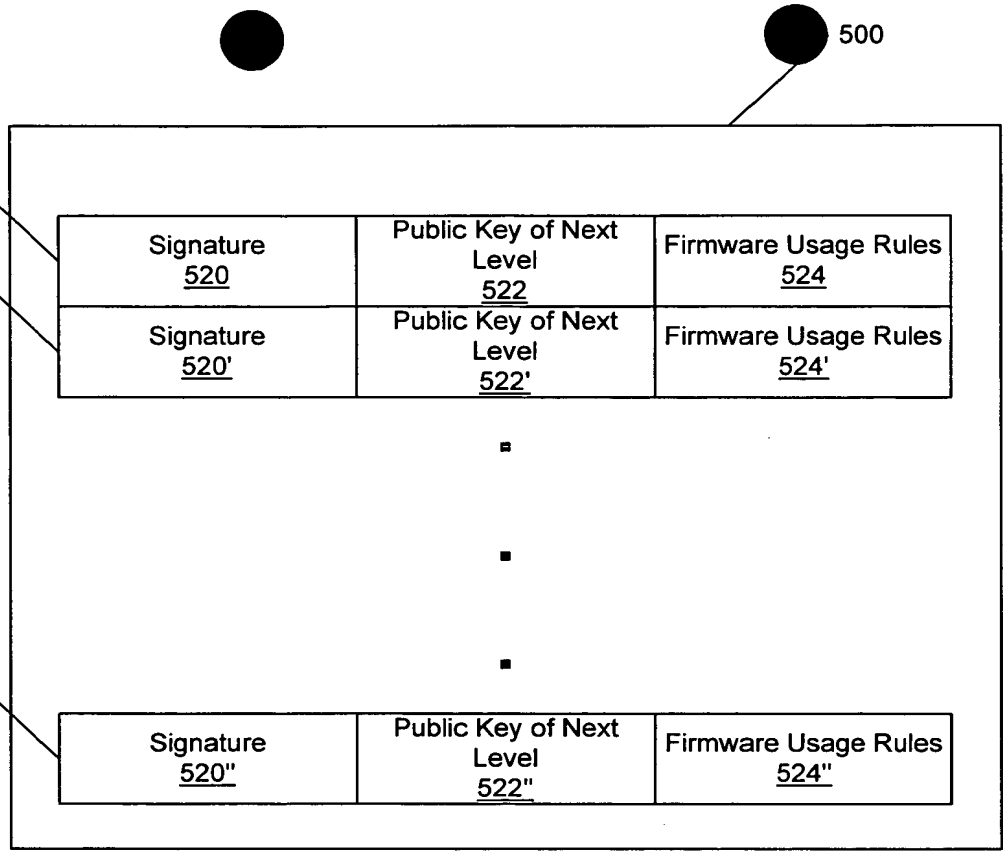


Figure 7

Figure 8

Figure 9

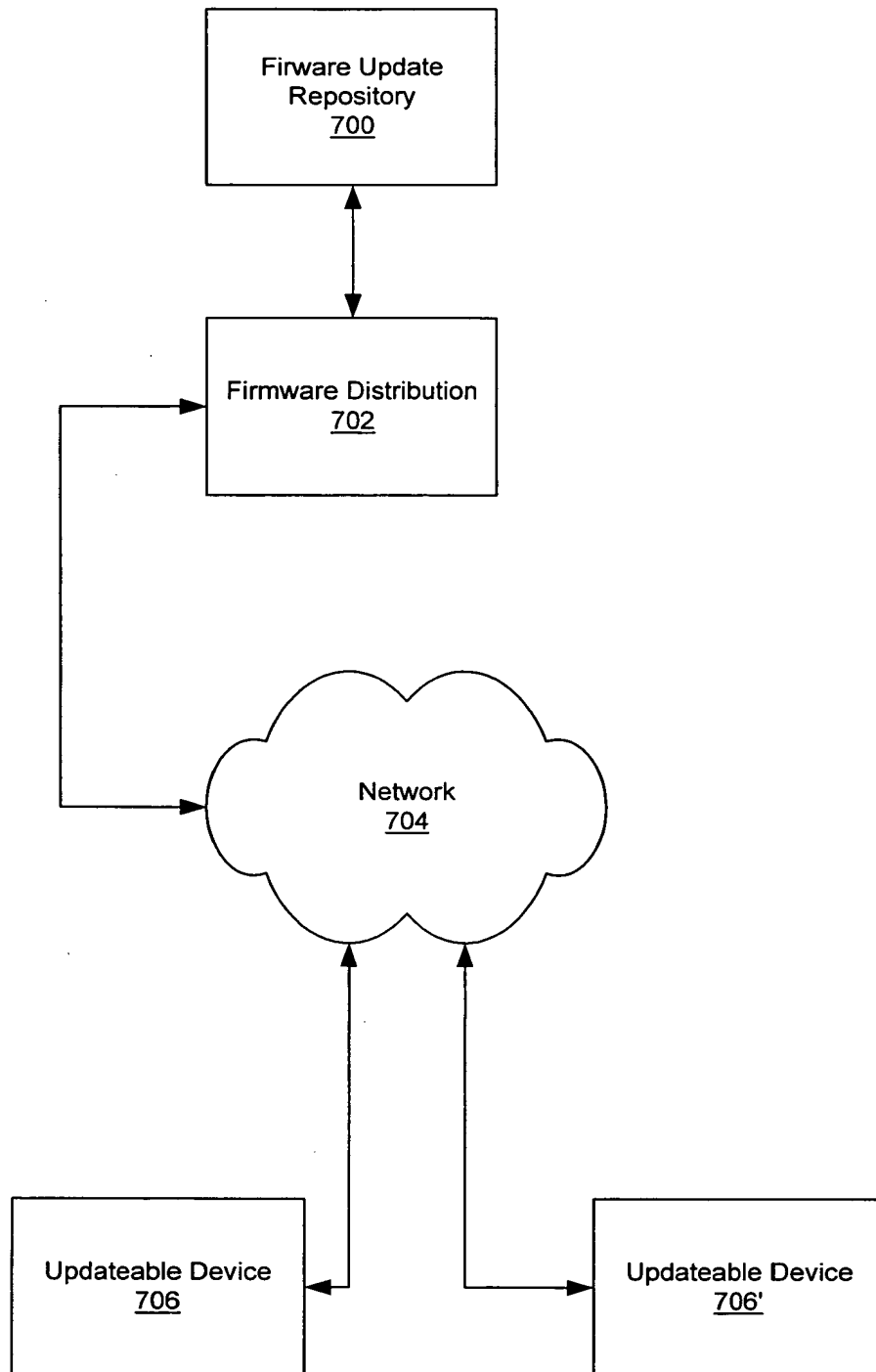


Figure 10

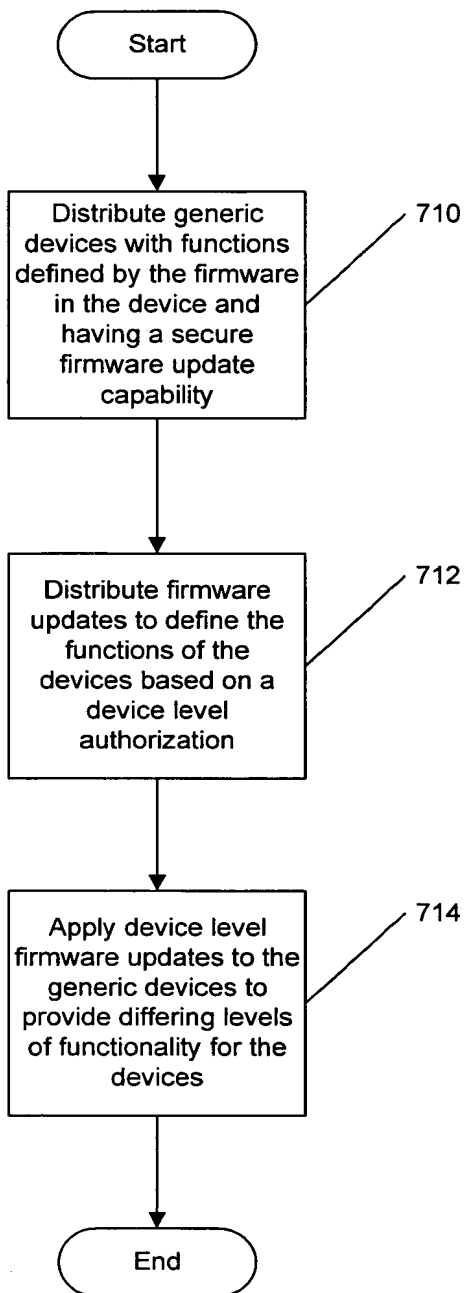


Figure 11